IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent Application

Applicant(s): Fernando et al.
Case: 11-18-8
Serial No.: 09/788,582
Filing Date: February 16, 2001
Group: 2115
Examiner: Chun Cao

I hereby certify that this paper is being deposited on this date with the U.S. Postal Service as first class mail addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450

Signature: [signature] Date: September 12, 2005

Title: Method and Apparatus for Transferring Multi-Source/Multi-Sink Control Signals Using a Differential Signaling Technique

---

TRANSMITTAL OF APPEAL BRIEF

Mail Stop Appeal Brief
Commissioner of Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Submitted herewith are the following documents relating to the above-identified patent application:

1. Appeal Brief; and
2. Copy of Notice of Appeal, filed on July 13, 2005, with copy of stamped return postcard indicating receipt of Notice by PTO on July 18, 2005.

There is an additional fee of $500 due in conjunction with this submission under 37 CFR §1.17(c). Please charge **Deposit Account No. 50-0762** the amount of $500, to cover this fee. In the event of non-payment or improper payment of a required fee, the Commissioner is authorized to charge or to credit **Deposit Account No. 50-0762** as required to correct the error. A duplicate copy of this letter is enclosed.

Respectfully,

[signature]

Date: September 12, 2005

Kevin M. Mason
Attorney for Applicant(s)
Reg. No. 36,597
Ryan, Mason & Lewis, LLP
1300 Post Road, Suite 205
Fairfield, CT 06824
(203) 255-6560

AF
ZFW

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent Application

Applicant(s): Fernando et al.
Case: 11-18-8
Serial No.: 09/788,582
Filing Date: February 16, 2001
Group: 2115
Examiner: Chun Cao

I hereby certify that this paper is being deposited on this date with the U.S. Postal Service as first class mail addressed to the Commissioner for Patents, P.O. 1450, Alexandria, VA 22313-1450

Signature: Gina Mauro Date: September 12, 2005

Title: Method and Apparatus for Transferring Multi-Source/Multi-Sink Control Signals Using a Differential Signaling Technique

---

APPEAL BRIEF

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicants hereby appeal the final rejection dated May 12, 2005, of claims 1 through 23 of the above-identified patent application.

REAL PARTY IN INTEREST

The present application is assigned to Agere Systems Inc., as evidenced by the statement under 37 CFR 3.73 (b) submitted on April 14, 2003. The assignee, Agere Systems Inc., is the real party in interest.

RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences.

STATUS OF CLAIMS

Claims 1 through 23 are pending in the above-identified patent application. Claims 1-23 remain rejected under 35 U.S.C. §102(b) as being anticipated by Tateishi (United States Patent Number 5,539,590). The disclosure is also objected to due to an indicated informality.

STATUS OF AMENDMENTS

There have been no amendments filed subsequent to the final rejection.

SUMMARY OF CLAIMED SUBJECT MATTER

The present invention is directed to a method and apparatus for transferring multi-source/multi-sink control signals using a differential signaling technique. An "active" state is transferred on a multi-source/multi-sink control signal network by inverting the previous voltage level, and an "inactive state" is transferred by maintaining the previous level (page 4, lines 21-25). A change in the voltage level associated with a given control signal indicates that at least one node on an SoC device is asserting the corresponding control signal (page 4, lines 25-27). In order to detect a change in the signal state from a previous cycle, each node includes a memory element, such as a latch, for maintaining the previous state. In this manner, a voltage level from the next interval can be compared to the recorded state to detect a change of state indicating an assertion of the control signal by another node. Thus, a given control signal is asserted whenever the state of the signal at the end of the previous cycle is different from the state of the signal at the end of the proceeding cycle. In one exemplary implementation, the asserted control signal is applied to an exclusive-OR gate together with the current value on the control signal wire to thereby cause a transition indicating an assertion of the control signal (page 5, lines 1-10; page 6, line 2, to page 9, line 6).

STATEMENT OF GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Claims 1-23 are rejected under 35 U.S.C. §102(b) as being anticipated by Tateishi.

ARGUMENT

Formal Objections

The disclosure is objected to due to an indicated informality. In particular, incorrect United States Patent Application numbers were cited as being related to the present invention. The Examiner was able to obtain the correct serial numbers from the patent application titles and properly identify the related patent applications. Applicants propose to correct the application numbers following resolution of the appeal.

Independent Claims 1, 8 and 16

Independent claims 1, 8, and 16 were rejected under 35 U.S.C. §102(b) as being anticipated by Tateisha. Regarding claim 1, the Examiner asserts that Tateisha discloses maintaining said voltage level of said control signal from the previous time interval to indicate a second signal state [no change of the floppy status]. In the response to arguments in the final Office Action, the Examiner acknowledges that "the signal STS is maintained at the high level as long as the floppy is in the floppy drive" and that "the signal STS is maintained at the low level as long as the floppy is not in the floppy drive."

Applicants note that Tateisha teaches that, regarding the status signal STS, a "low level (is) indicative of the unloaded state." (Col. 7, lines 54-55.) Consequently, as the Examiner acknowledges, a high level is indicative of a loaded state. Thus, the signal STS does not indicate a *first signal state by adjusting a voltage level from a previous time interval*; and indicate *a* ***second signal state by maintaining the voltage level from the previous time interval.***

Also, as the Examiner notes, a change in the state of the STS signal (either from a low level to a high level, or from a high level to a low level) causes the output of EX1 to transition from a low level to a high level (see, FIG. 3). Following the next transition of clock CK, the new level of the status signal STS will propagate to the output of the flip-flop in recovery controller 21j and the output of EX1 will transition from the high level back to a low level. The transition of the output from EX1 from the high level back to a low level ***will occur even if the status signal does not change again.*** Thus, a single change of state of the status signal STS will result in ***two*** voltage changes of the output of EX1; one of the voltage changes occurs when there is no change of the floppy status. The output of EX1, therefore, does not maintain the voltage of a control signal to indicate no change of the floppy status. Independent claim 1 requires maintaining said voltage level of said control signal from the previous time interval to indicate a second signal state. Independent claim 8 requires detecting a second signal state if said voltage level from the previous time interval is maintained. Independent claim 16 requires a memory element for maintaining a voltage level from a previous time interval.

Conclusion

Thus, Tateisha does not disclose or suggest maintaining said voltage level of said control signal from the previous time interval to indicate a second signal state, as required by

independent claim 1, does not disclose or suggest detecting a second signal state if said voltage level from the previous time interval is maintained, as required by independent claim 8, and does not disclose or suggest a memory element for maintaining a voltage level from a previous time interval, as require by independent claim 16.

The rejections of the independent claims under section §102 in view of Tateisha, alone or in any combination, are therefore believed to be improper and should be withdrawn. The remaining rejected dependent claims are believed allowable for at least the reasons identified above with respect to the independent claims.

The attention of the Examiner and the Appeal Board to this matter is appreciated.

Respectfully,

Date: September 12, 2005

Kevin M. Mason
Attorney for Applicant(s)
Reg. No. 36,597
Ryan, Mason & Lewis, LLP
1300 Post Road, Suite 205
Fairfield, CT 06824
(203) 255-6560

APPENDIX

1. A method for transmitting a control signal on a bus, said control signal having two signal states, said method comprising the steps of:

adjusting a voltage level of said control signal from a previous time interval to indicate a first signal state; and

maintaining said voltage level of said control signal from the previous time interval to indicate a second signal state.

2. The method of claim 1, further comprising the step of maintaining said voltage level from the previous time interval using a memory element.

3. The method of claim 1, further comprising the step of ensuring that only a single node connected to said bus can assert said control signal in a given time interval.

4. The method of claim 1, wherein said bus is on a system-on-chip.

5. The method of claim 1, wherein said bus is on a printed circuit board.

6. The method of claim 1, wherein said adjusting step further comprises the step of transitioning from a first voltage level to a second voltage level.

7. The method of claim 1, wherein said adjusting step further comprises the step of applying a high logic level to an exclusive-OR gate with said voltage level from the previous time interval to determine the signal level to be asserted in the current time interval.

8. A method for receiving a control signal on a bus, said control signal having two signal states, said method comprising the steps of:

detecting a first signal state for said control signal if a voltage level from a previous time interval is adjusted; and

detecting a second signal state if said voltage level from the previous time interval is maintained.

9. The method of claim 8, further comprising the step of maintaining said control signal value at said voltage level from said previous time interval when no node drives said bus.

10. The method of claim 9, further comprising the step of compensating for leakage and cross-coupling effects.

11. The method of claim 8, further comprising the step of maintaining said voltage level from the previous time interval using a memory element.

12. The method of claim 8, wherein said bus is on a system-on-chip.

13. The method of claim 8, wherein said bus is on a printed circuit board.

14. The method of claim 8, wherein said adjusted voltage level is a transitioning from a first voltage level to a second voltage level.

15. The method of claim 8, wherein said first detecting step further comprises the step of applying said received control signal state to an exclusive-OR gate with said voltage level from the previous time interval to determine the signal level to be asserted in the current time interval.

16. A device for communicating a control signal on a bus, said control signal having two signal states, said device comprising:

a memory element for maintaining a voltage level from a previous time interval;

a comparison circuit for detecting a change in said voltage level from the previous time interval indicating an assertion of said control signal by another device; and

an adjustment circuit for changing said voltage level from the previous time interval indicating an assertion of said control signal by another device.

17. The device of claim 16, wherein said memory element is a latch.

18. The device of claim 16, further comprising a circuit that ensures that only a single device connected to said bus can assert said control signal in a given time interval.

19. The device of claim 16, wherein said bus is on a system-on-chip.

20. The device of claim 16, wherein said bus is on a printed circuit board.

21. The device of claim 16, wherein said change in said voltage level from the previous time interval is a change from a first voltage level to a second voltage level.

22. The device of claim 16, wherein said adjustment circuit is an exclusive-OR gate.

23. The device of claim 16, wherein said comparison circuit is an exclusive-OR gate.

EVIDENCE APPENDIX

There is no evidence submitted pursuant to § 1.130, 1.131, or 1.132 or entered by the Examiner and relied upon by appellant.

RELATED PROCEEDINGS APPENDIX

There are no known decisions rendered by a court or the Board in any proceeding identified pursuant to paragraph (c)(1)(ii) of 37 CFR 41.37.